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CLAIMS

1. A method of continuously tuning a transconductance comprising:

coupling a degeneration resistance from a first source of a first transistor in a differential pair of transistors to a second source of a second transistor in the differential pair of transistors:

applying a second variable degeneration resistance in parallel to the first degeneration resistance in response to the application of a first variable control voltage; and

applying a third variable degeneration resistance in parallel to the first degeneration resistance and the second degeneration resistance in response to the application of a second variable control voltage having a fixed voltage offset from the first variable control voltage.

2. The method of continuously tuning a transconductance of claim 1, in which application of the first and second variable degeneration resistances comprises applying the first and the second variable control voltages to a gate connection of a first NMOS transistor and a second NMOS transistor respectively such that a channel of the first NMOS transistor and a channel of the second NMOS transistors form a variable degeneration resistance.

3. A voltage to current converter for producing a variable transconductance comprising:

a variable degeneration resistance;

a differential pair of transistors having a first transistor coupled to a first terminal of the variable degeneration resistance and a second transistor coupled to a second terminal of the variable degeneration resistance; and

a voltage offset ladder circuit producing a plurality of voltages in a fixed offset relationship to each other coupled to the

variable degeneration resistance in order to control the transconductance of the variable gain amplifier.

4. The variable gain amplifier of claim 3, further comprising a substrate upon which the variable gain amplifier is disposed.

5. The variable gain amplifier of claim 3, in which the voltage offset ladder circuit couples a control voltage to the variable degeneration resistance and couples the control voltage including an offset voltage to the variable degeneration resistance.

6. The variable gain amplifier of claim 3, in which the variable degeneration resistance includes a first terminal coupled to a source of the first transistor of the differential pair of transistors and a second terminal coupled to a source of the second transistor of the differential pair of transistors.

7. The variable gain amplifier of claim 3, in which the differential pair of transistors are NMOS devices.

8. A variable gain amplifier system comprising:
a variable gain amplifier producing a variable gain in response to a control voltage;
a control circuit accepting an AGC control signal and producing a plurality of control voltages, offset in voltage from each other, and having each of the plurality of control voltages coupled to the variable gain amplifier.

9. An integrated communications system comprising:
a substrate;
a receiver disposed upon the substrate and converting an incoming RF signal to an IF signal;

a variable gain amplifier disposed upon the substrate cascaded after the receiver having the IF signal as an input and having a gain responsive to a strength of the incoming RF signal, the variable gain amplifier having,

a first transistor having a source coupled to a first terminal of a first current source, a drain coupled to a first terminal of a differential output, and a gate coupled to a first terminal of a differential input, and the first current source having a second terminal coupled to ground;

a second transistor having a source coupled to a first terminal of a second current source, a drain coupled to a second terminal of the differential output, and a gate coupled to a second terminal of the differential input, and the second current source having a second terminal coupled to ground;

a variable degeneration resistance having a first and a second output terminal wherein the first output terminal of the variable degeneration resistance couples to the source of the first transistor to the drain of a first degeneration transistor, the second output terminal of the variable degeneration resistance couples to the source of the second transistor to the source of a first degeneration transistor, and a gate of the first degeneration transistor forming a first control voltage input, and wherein the drain of the first degeneration transistor is coupled to a first terminal of a first resistor, and a second terminal of the first resistor is coupled to a first terminal of a second resistor and in parallel to a drain of a second degeneration transistor, a source of the second degeneration transistor is coupled to a first terminal of a third resistor and to a second terminal of a fourth resistor, a first terminal of the fourth resistor is coupled to the source of the first degeneration transistor, the second degeneration transistor having a gate forming a second control voltage input, and wherein

a second terminal of the second resistor is coupled to a second terminal of the third resistor; and

a voltage offset ladder circuit having a control voltage input coupled to the second control voltage input of the variable degeneration resistance, and to a first terminal of a first voltage offset resistor, and having a second terminal of the first voltage offset resistor coupled to the first control voltage input of the variable degeneration resistance, and to a first terminal of an offset current source, and having a second terminal of the offset current source coupled to a ground.

10. The integrated communications system of claim 9, in which:

the first transistor is an NMOS transistor;

the second transistor is an NMOS transistor;

the first degeneration transistor is an NMOS transistor; and

the second degeneration transistor is an NMOS transistor.

11. A method of producing a variable gain current output signal in a differential pair amplifier having a control voltage input to a voltage offset ladder circuit controlling a variable impedance, the variable impedance including a plurality of degeneration resistance circuits, and having the variable impedance coupled to a differential pair amplifier, comprising:

applying a control voltage to a first degeneration resistance circuit;

superimposing a voltage offset on to the control voltage in the voltage offset ladder to form a first offset control voltage;

applying the first offset control voltage to a second degeneration resistance circuit; and

coupling the variable impedance, including the plurality of degeneration resistance circuits, to the differential pair amplifier.

12. A method of varying the gain of a differential pair amplifier comprising:

coupling a first degeneration resistance to a differential pair amplifier in response to an applied control voltage; and

applying a second degeneration resistance to the differential pair amplifier in response to an increase in the applied control voltage.

13. A variable gain amplifier having a variable transconductance comprising:

a first transistor having a source coupled to a first terminal of a first current source, a drain coupled to a first terminal of a differential output, and a gate coupled to a first terminal of a differential input, and the first current source having a second terminal coupled to ground;

a second transistor having a source coupled to a first terminal of a second current source, a drain coupled to a second terminal of the differential output, and a gate coupled to a second terminal of the differential input, and the second current source having a second terminal coupled to ground;

a variable degeneration resistance having a first and a second output terminal wherein the first output terminal of the variable degeneration resistance couples to the source of the first transistor to the drain of a first degeneration transistor, the second output terminal of the variable degeneration resistance couples to the source of the second transistor to the source of a first degeneration transistor, and a gate of the first degeneration transistor forming a first control voltage input, and wherein the drain of the first degeneration transistor is coupled to a first terminal of a first resistor, and a second terminal of the first resistor is coupled to a first terminal of a second resistor and in parallel to a drain of a second degeneration transistor, a source of the second

degeneration transistor is coupled to a first terminal of a third resistor and to a second terminal of a fourth resistor, a first terminal of the fourth resistor is coupled to the source of the first degeneration transistor, the second degeneration transistor having a gate forming a second control voltage input, and wherein a second terminal of the second resistor is coupled to a second terminal of the third resistor; and

a voltage offset ladder circuit having a control voltage input coupled to the second control voltage input of the variable degeneration resistance, and to a first terminal of a first voltage offset resistor, and having a second terminal of the first voltage offset resistor coupled to the first control voltage input of the variable degeneration resistance, and to a first terminal of an offset current source, and having a second terminal of the offset current source coupled to a ground.

14. The variable gain amplifier of claim 13, further comprising a substrate.

15. The variable gain amplifier of claim 14, in which the substrate is fabricated according to the n-well CMOS process.

16. The variable gain amplifier of claim 13, in which the first transistor, the second transistor, the first degeneration transistor, and the second degeneration transistor are each NMOS devices each having a backgate terminal coupled to a ground connection.

17. An integrated communications system comprising:
a substrate;
a receiver disposed upon the substrate and converting an incoming RF signal to an IF signal;

a variable gain amplifier disposed upon the substrate cascaded after the receiver having the IF signal as an input and having a gain responsive to a strength of the incoming RF signal, the variable gain amplifier having,

a first transistor having a source coupled to a first terminal of a first current source, a drain coupled to a first terminal of a differential output, and a gate coupled to a first terminal of a differential input;

a second transistor having a source coupled to a first terminal of a second current source, a drain coupled to a second terminal of the differential output, and a gate coupled to a second terminal of the differential input;

a variable degeneration resistance having a first and a second output terminal wherein the first output terminal of the variable degeneration resistance couples to the source of the first transistor to the drain of a first degeneration transistor, the second output terminal of the variable degeneration resistance couples to the source of the second transistor to the source of a first degeneration transistor, and a gate of the first degeneration transistor forming a first control voltage input, and wherein the drain of the first degeneration transistor is coupled to a first terminal of a first resistor, and a second terminal of the first resistor is coupled to a first terminal of a second resistor and in parallel to a drain of a second degeneration transistor, a source of the second degeneration transistor is coupled to a first terminal of a third resistor and to a second terminal of a fourth resistor, a first terminal of the fourth resistor is coupled to the source of the first degeneration transistor, the second degeneration transistor having a gate forming a second control voltage input, and wherein a second terminal of the second resistor is coupled to a second terminal of the third resistor; and

a voltage offset ladder circuit having a control voltage input coupled to the second control voltage input of the variable degeneration resistance, and to a first terminal of a first voltage offset resistor, and having a second terminal of the first voltage offset resistor coupled to the first control voltage input of the variable degeneration resistance, and to a first terminal of an offset current source.

18. A variable gain amplifier having a variable transconductance comprising:

a first transistor having a source coupled to a first terminal of a first current source, a drain coupled to a first terminal of a differential output, and a gate coupled to a first terminal of a differential input;

a second transistor having a source coupled to a first terminal of a second current source, a drain coupled to a second terminal of the differential output, and a gate coupled to a second terminal of the differential input;

a variable degeneration resistance having a first and a second output terminal wherein the first output terminal of the variable degeneration resistance couples to the source of the first transistor to the drain of a first degeneration transistor, the second output terminal of the variable degeneration resistance couples to the source of the second transistor to the source of a first degeneration transistor, and a gate of the first degeneration transistor forming a first control voltage input, and wherein the drain of the first degeneration transistor is coupled to a first terminal of a first resistor, and a second terminal of the first resistor is coupled to a first terminal of a second resistor and in parallel to a drain of a second degeneration transistor, a source of the second degeneration transistor is coupled to a first terminal of a third resistor and to a second terminal of a fourth resistor, a first

terminal of the fourth resistor is coupled to the source of the first degeneration transistor, the second degeneration transistor having a gate forming a second control voltage input, and wherein a second terminal of the second resistor is coupled to a second terminal of the third resistor; and

a voltage offset ladder circuit having a control voltage input coupled to the second control voltage input of the variable degeneration resistance, and to a first terminal of a first voltage offset resistor, and having a second terminal of the first voltage offset resistor coupled to the first control voltage input of the variable degeneration resistance, and to a first terminal of an offset current source.